In the drawings:

In Figure 1A please insert the words "Prior Art" as indicated in the replacement sheet.

In Figure 1B, please insert the words "Prior Art" as indicated in the replacement sheet.

Remarks

Claims 1-11 are presently pending. Claims 1-6 and 8-11 are presently pending and stand rejected.

The drawings were objected to. Assignee presents Examiner with replacement drawings and requests substitution of the original drawings with the replacement drawings. Assignee respectfully submits that the replacement drawings overcome the objections and do not include new subject matter.

Claim 1 was rejected under 35 U.S.C. 102(b) as anticipated by U.S. Patent 5,572,710 ("Asano"). Asano is directed to "A high speed logic simulation system using time division emulation suitable for large scale logic circuits". Asano, Title.

In Asano, "the mapping data are down loaded from the host computer i through the host interface 3 and the emulation controller 8 to the network 5, the emulation chips 6, and the memory module 7 of the emulator 4. Here, the emulation chips 6 and the memory module 7 are mutually interconnected by the network 5 to emulate the simulation target, where the memory module 7 is used for emulating the memory portion such as SRAM, DRAM, etc. contained in the simulation target." Asano, Col. 7, Lines 55-63 (Emphasis Added).

Examiner has indicated that "Asano discloses a hardware emulator for verifying a plurality of systems on chip, said emulator comprising: a first circuitry for verifying a first system on chip; and a second circuitry for verifying a second system on chip while verifying the first system on chip (col. 7 lines 55-63, Fig. 2)." Office Action, p. 5.

Assignee respectfully submits that Asano, col. 7, lines 55-63, teach to emulate, merely, "the simulation target" and "emulating the memory portion such as SRAM, DRAM, etc. contained in the simulation target." Assignee calls particular attention to the use of the singular context. Thus, Assignee respectfully submits that the Asano does not teach or fairly suggest the claimed "verifying a second system on chip while verifying the first system on chip". However, in the interests of clarity, Assignee has amended claim 1 to recite "while verifying a second system on another chip" and submits that Asano does not teach or fairly

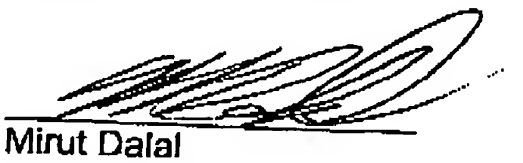
suggest claim 1 as amended. Accordingly, Examiner is requested to withdraw the rejection to claim 1 and dependent claims 2 and 3. Similarly, Examiner is requested to withdraw the rejection under 35 U.S.C. 102(b) to claims 4-6, and 35 U.S.C. 103(a) to claims 8-11 (the obviousness rejection relies on Asano alleged teaching).

Claim 6 was rejected under 35 U.S.C. 101. Assignee has amended claim 6 and cancelled claim 7. It is repectfully submitted that claim 6 as now amended overcomes this rejection. Claims 10 and 11 were rejected under 35 U.S.C. 101 and have been amended to set forth the useful, concrete, and real world result, "configuring a hardware emulator". It is respectfully submitted that claims 10 and 11, as amended, overcome this rejection.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Date: August 21, 2006

Respectfully submitted,



Mirut Dalal
ATTORNEY FOR ASSIGNEE
Reg. No. 44,052

McAndrews, Held & Malloy, Ltd.
500 West Madison – Suite 3400
Chicago IL 60661

Phone (312) 775-8000
FAX (312) 775-8100